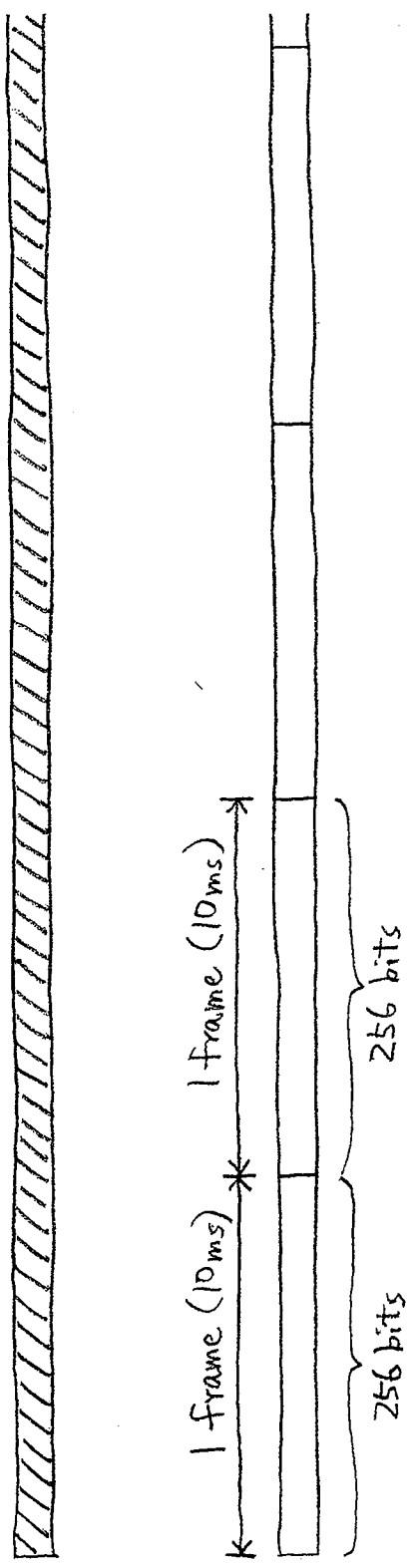
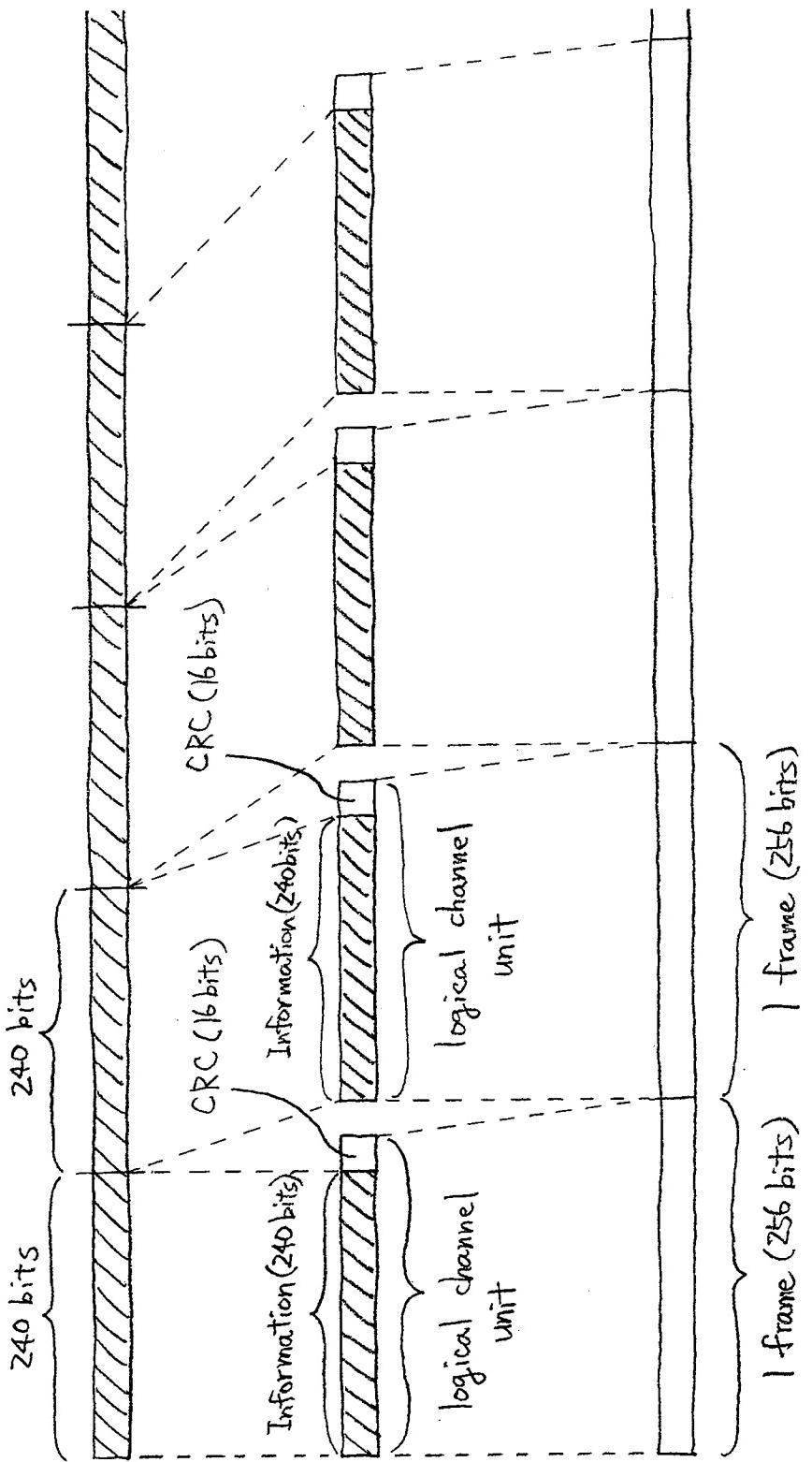


APPENDIX

(a) Information of logical channel

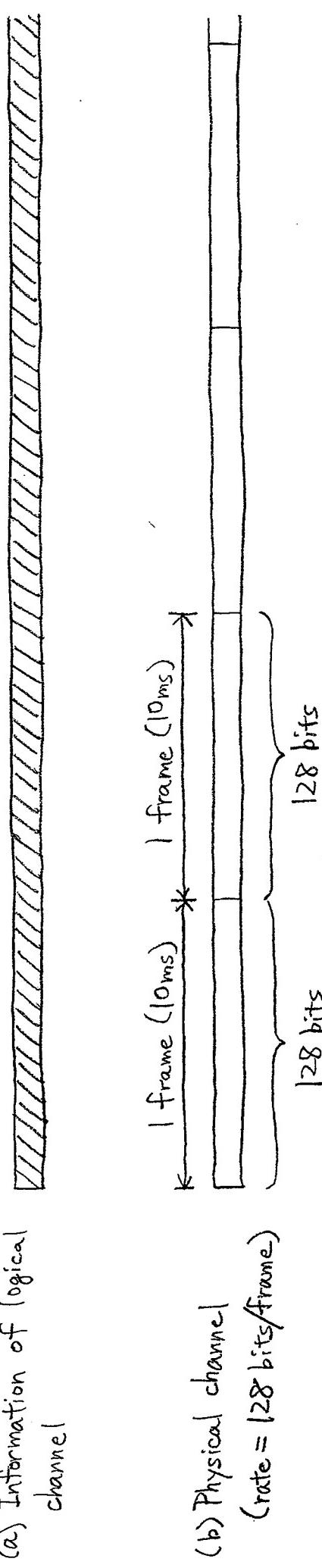


(b) Physical channel
(rate = 256 bits/frame)



Reference Figure 1

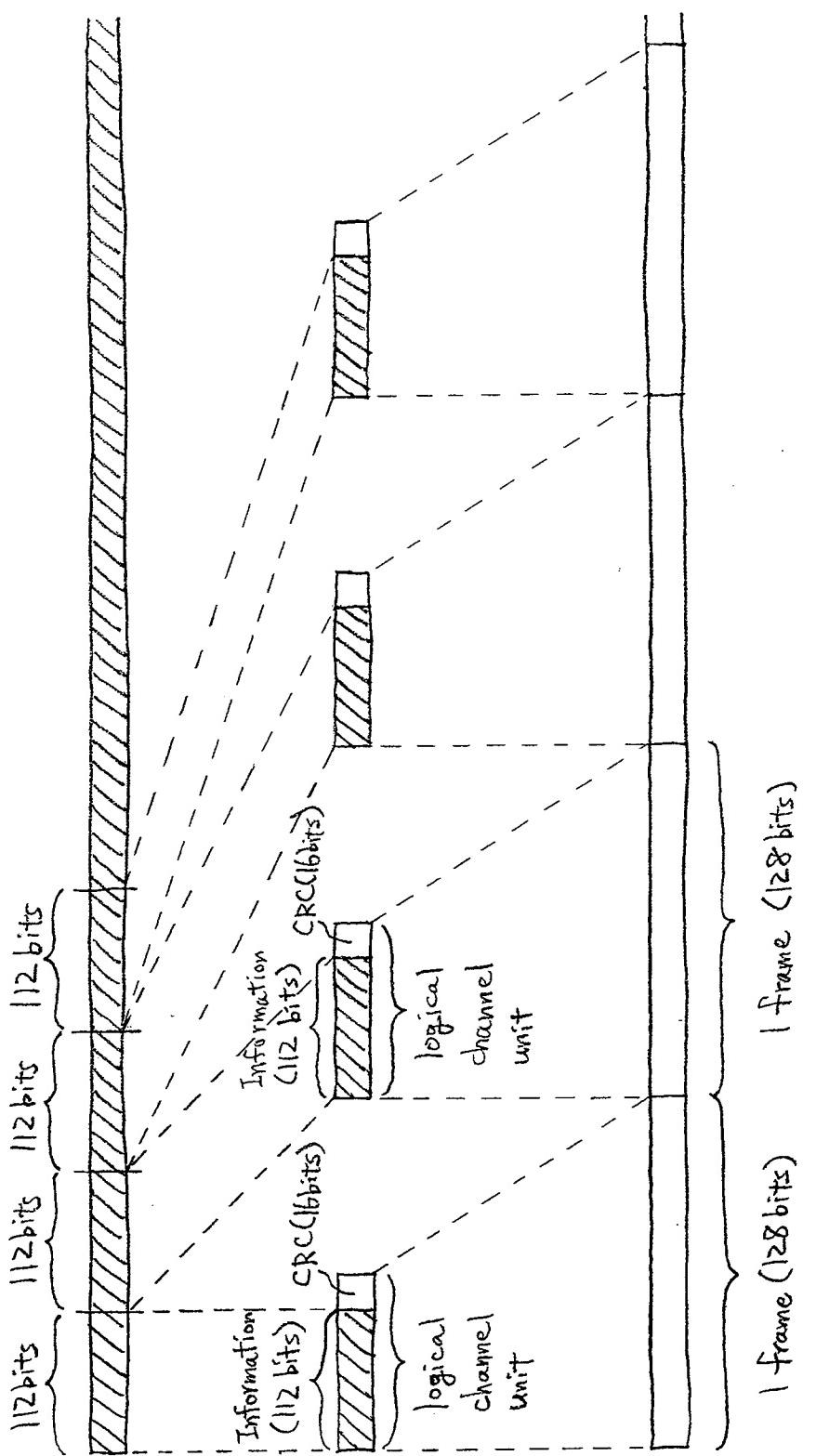
(a) Information of logical channel



(i) Dividing information of logical channel into segments each of which has $128 - 16 = 112$ bits

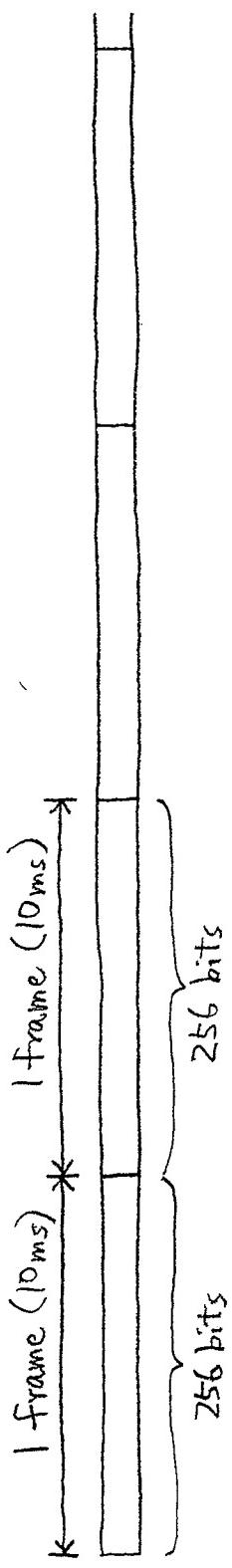
- (ii) Forming each logical channel unit by adding CRC (16 bits) to each information segment

(iii) Mapping logical channel into physical channel

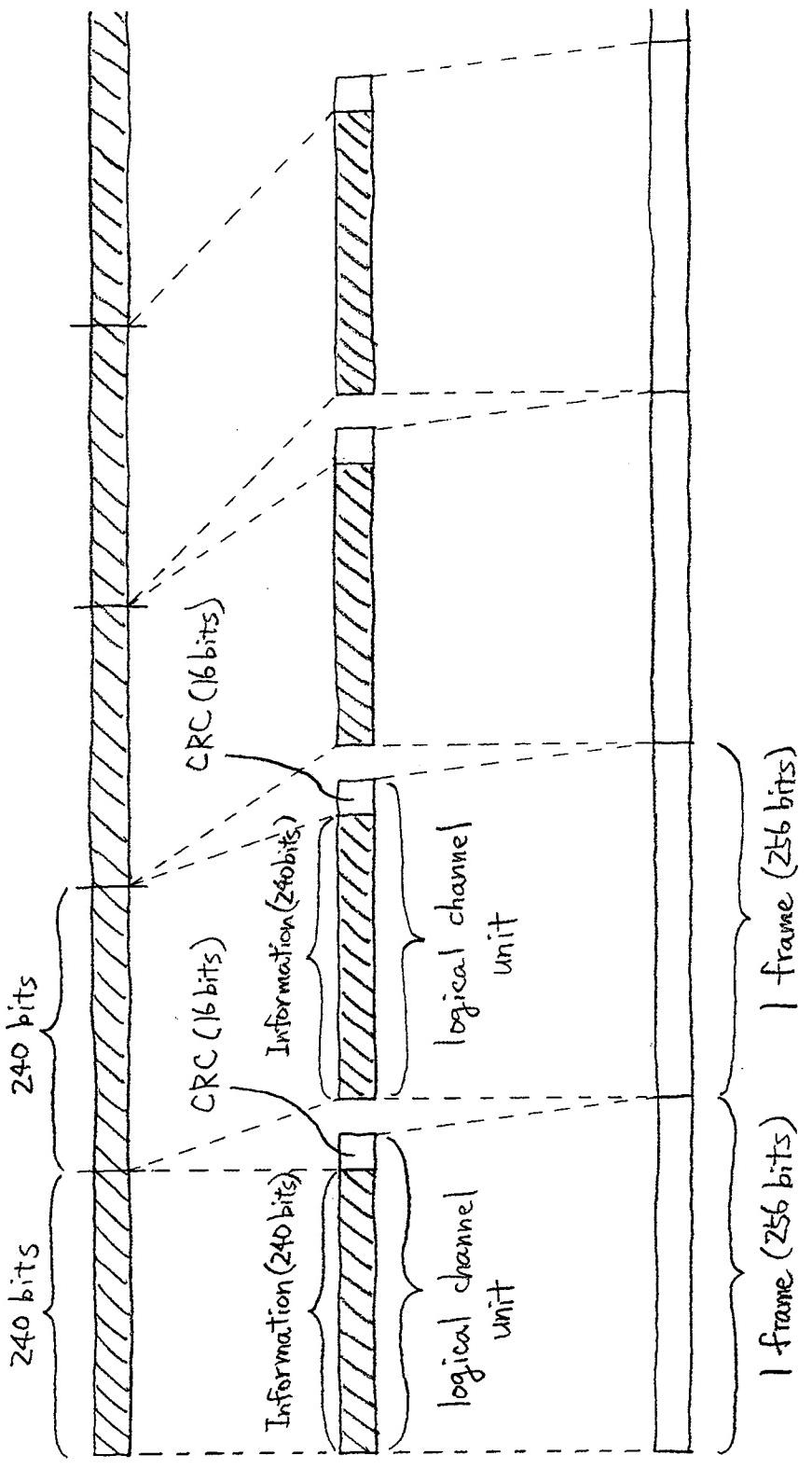


Reference Figure 2

(a) Information of logical channel



(i) Dividing information of logical channel into segments each of which has $256 - 16 = 240$ bits



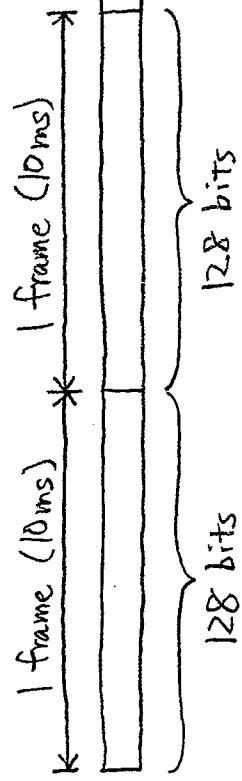
(ii) Forming each logical channel unit by adding CRC (16 bits) to each information segment

(iii) Mapping logical channel into physical channel

Reference Figure 3

(a) Information of logical channel

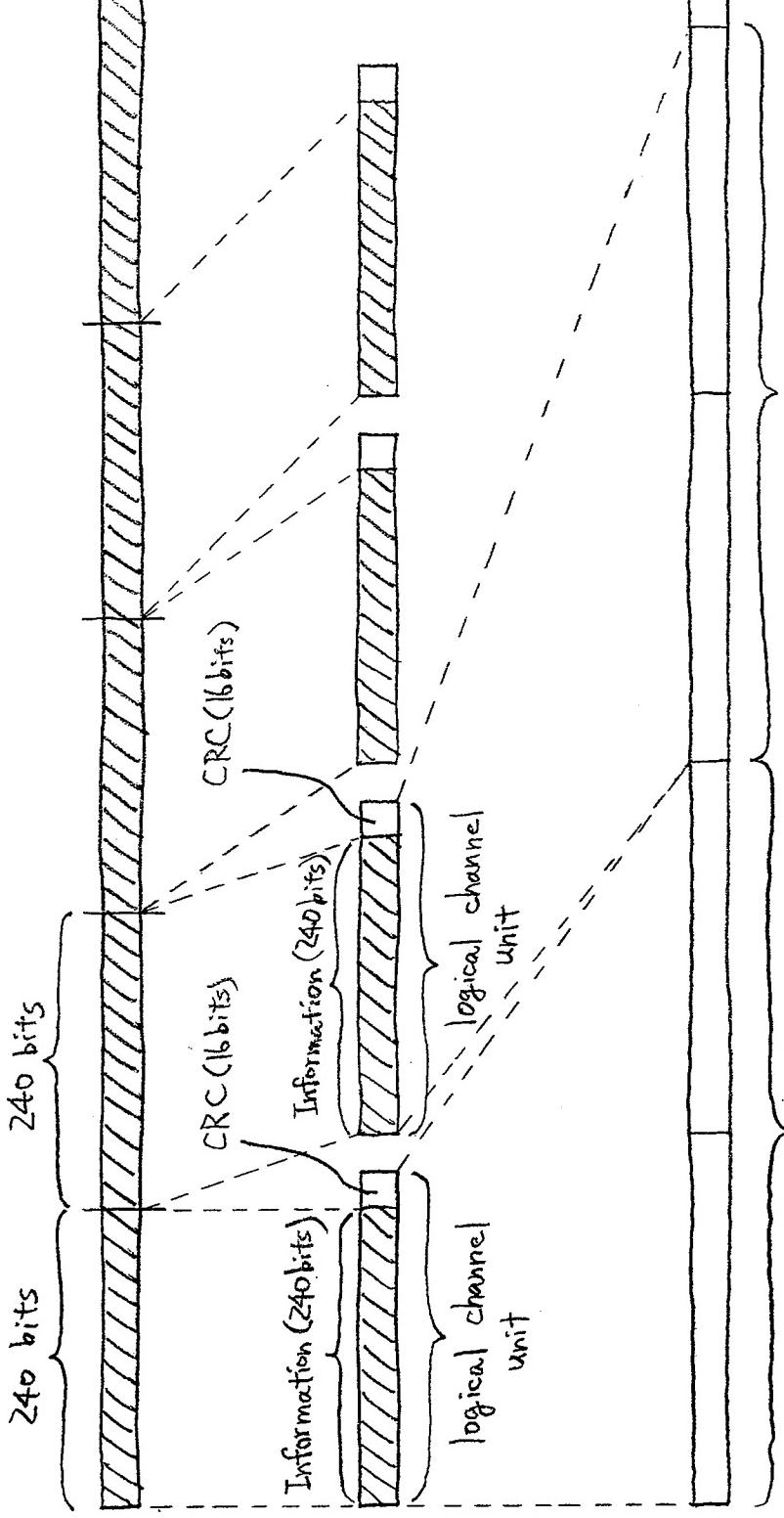
(b) Physical channel
(rate = 128 bits/frame)



(i) Dividing information of logical channel into segments each of which has $128 + 16 - 16 = 240$ bits

(ii) Forming each logical channel unit by adding CRC (16 bits) to each information segment

(iii) Mapping logical channel into physical channel



Reference Figure 4

2 frames (128+128=256 bits)

2 frames (128+128=256 bits)